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embodiment of the present invention each comprises an instruction fetch unit 54-59 connected to the memory 12, an instruction issue unit 80-85 connected to the instruction fetch unit 54-59, instruction execution units LU0, IU0, IU1, FU0, FU1, MU0, MU1, and BU0, and a register unit 100 connected to all the instruction execution units. Here, the instruction execution units MU0 and MU1 are special-purpose arithmetic instruction execution units that execute special-purpose arithmetic instructions. When the execution of special-purpose arithmetic instructions is completed, the instruction execution units MU0 and MU1 notify the instruction issue unit 80-85 of the end of the execution.

Please REPLACE the paragraph beginning at page 35, line 8, with the following paragraph:

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In the following, the parallel processors in accordance with the third embodiment of the present invention will be described by way of a case where the maximum basic instruction word length contained in one instruction word is 2. It should be understood that the same effects can be obtained in a case where the maximum instruction word length contained in one instruction word is 3 or more.

IN THE CLAIMS:

Please AMEND the claims in accordance with the following:

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1. A parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information, said parallel processor comprising:

a plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel;

an instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information; and

an instruction issue unit recognizing and, in accordance therewith, selectively issuing each of the basic instructions supplied from the instruction fetch unit to one of the

corresponding instruction execution units to execute the issued basic instruction.

7. The parallel processor as claimed in claim 1, wherein, depending on the type of a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of the basic instruction being currently executed is completed.

Please ADD the following new claims:

9. The parallel processor as claimed in claim 1, wherein the instruction issue unit further comprises an interface corresponding to the instruction execution units indicating whether the corresponding instruction execution unit is available.

10. A parallel processor as claimed in claim 9, wherein the instruction issue unit further comprises a table for setting effective bits to indicate availability of the corresponding instruction execution unit.

11. A parallel processor as claimed in claim 10, wherein a first instruction word format is converted into a second instruction word format by the table, the first instruction word format indicating an arrangement of instruction words from the instruction fetch unit, and the second instruction word format indicating an arrangement of instruction words which corresponds to the instruction execution units.

12. A parallel processor as claimed in claim 9, wherein the instruction issue unit further comprises a conversion unit for converting a first instruction word format into a second instruction word format on the basis of effective bits, corresponding to the instruction execution units, indicating whether the corresponding instruction execution unit is available.

13. A parallel processor as claimed in claim 12, wherein the first instruction word format indicates an arrangement of instruction words from the instruction fetch unit, and the second instruction word format indicates an arrangement of instruction words which corresponds to the instruction execution units.

14. A parallel processor performing parallel processing of one or more basic